1. (Twice Amended) A method of adjusting a local clock of a digital data decoder, wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, the method comprising the steps of :

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero; including the steps of:

i) using the hardware to adjust the local clock frequency until a threshold condition occurs, and

ii) after the threshold condition occurs, using the processor to adjust the local clock frequency.

3. (Once Amended) A method of adjusting a local clock of a digital data decoder, wherein the clock oscillates at a local clock frequency, the method further comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify the program clock value and frequency;

maintaining a program clock value based on the clock signals received at the decoder;

C3 cont.

determining if there is any difference between the local clock and the program clock frequencies;

determining if there is an absolute difference between the local clock value and the program clock value;

B3

if there is either a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and

wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the processor to adjust the local clock frequency.

Sub E3

7. (Once Amended) A system for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

means for maintaining a local clock value based on the oscillations of the local clock;

means for receiving clock signals transmitted to the decoder at a program clock frequency;

means for maintaining a program clock value based on the clock signals transmitted to the decoder;

E3

means for determining if there is any difference between the local clock and the program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value, so that said difference approaches zero;

wherein the means for adjusting the frequency at which the local clock oscillates includes:

hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processor having a software program for adjusting the local clock frequency after the threshold condition occurs.

13. A system for adjusting a local clock of a digital data decoder, comprising:

means for determining if there is any difference between the local and program clock frequencies;

means for determining if there is an absolute difference between the local clock value and the program clock value; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock values, or an absolute difference between the local clock value and the program value, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.